A 35 GHZ MONOLITHIC MESFET LNA

S.Bandla, G.Dawe, C.Bedard, R.Tayrani
D.Shaw, L.Raffaelli, and R.Goldwasser

GAMMA MONOLITHICS
A partnership between Martin Marietta Corporation and Alpha Industries, Inc.
20 Sylvan Road
Woburn, MA 01801

ABSTRACT

This paper describes the design and fabrication of a state of the art 35 GHz Monolithic Amplifier. The amplifier with 6.5 dB gain, 4 dB noise figure and 10 dBm power output at 1 dB gain compression is based on a .25x200 micron MBE grown MESFET. Device, circuit design, fabrication details and test results are presented.

INTRODUCTION

State of the art millimeter wave low noise amplifier performance has been achieved using the production preferred MESFET technology and the measured performance now rivals previously published HEMT results (1). The material producibility and compatibility for high level integration strongly favors MESFET technology for system level integration and costs. In this paper, we present in detail the design and fabrication of a Ka-band monolithic LNA using advanced MESFET technology.

DEVICE DESIGN

The 0.25 um gate length MESFET devices were fabricated on high quality MBE materials. The material structure consist of 500A N+ cap layer doped to 3 x 10^{18} cm^{-3}, 1000A of channel layer doped to 6 x 10^{17} cm^{-3} and one micron undoped GaAs buffer layer grown on LEC semi-insulating GaAs substrate.

The device geometry as shown in Figure 1, consists of six unit gate widths of 33.3 microns with three gate feeds connected by airbridges to the central gate pad. The source pads are grounded through via hole to maximize device gain at millimeter wave band.

The device R.F. model was obtained by fitting measured S-parameter data through 26.5 GHz from on wafer probe measurements. The equivalent circuit shown in Figure 2 illustrates the final element values for this model. The initial values were obtained from the combination of device theoretical analysis and DC measurement techniques utilizing computer aided design tools. CAD optimization technique was used to accurately fit the measured data. Based on this model, f_t = 32 GHz and f_{max} = 95 GHz were obtained.

FABRICATION

The circuits were fabricated on MBE material comprised of a silicon doped N+ cap and an active N layer on an undoped buffer.

At the mesa level, a standard wet etch process was employed to isolate devices and establish resistors.

The AuGe/Ni/Au ohmic contact formed a smooth topography for source/drain structures.

Gate level was defined by E-Beam direct write lithography. Gate recess and Schottky metal lift-off yielded a .27 micron gate length.

MIM capacitors were structured with Ti Pt Au and Si_3N_4. The airbridges, transmission lines and bonding pads were Au plated to 3 microns.

Via's were isotropically etched and also plated to 3 microns.

CIRCUIT DESIGN

Since the system application is for radar with less than 10% fractional bandwidth, a single frequency reactance matching technique was chosen. The linear element model (Fig. 2) is extrapolated to obtain S-parameters up to Ka-band.

For the first iteration design, the goal was to obtain maximum gain with the

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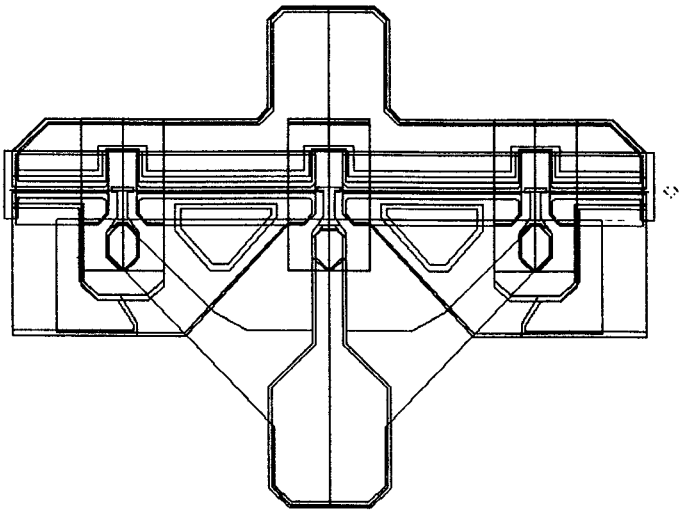
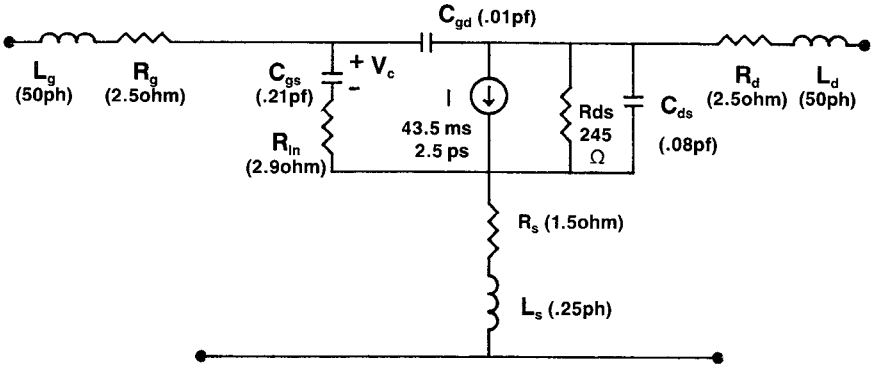
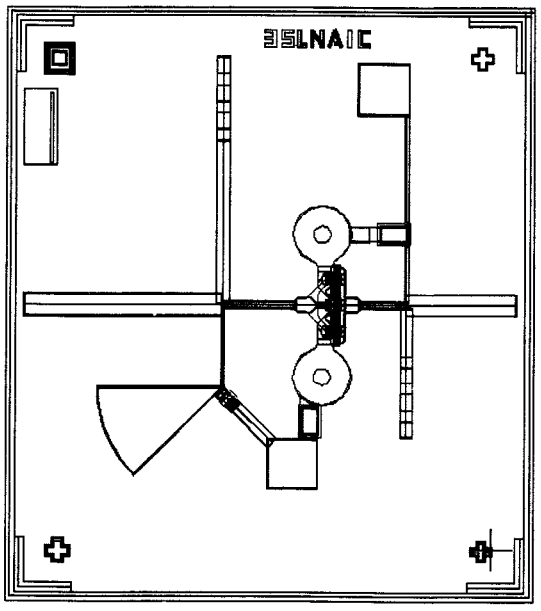


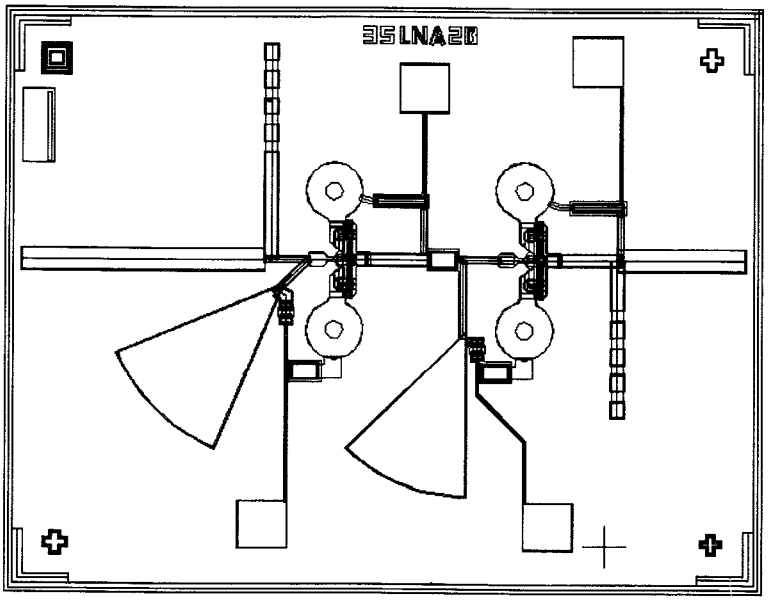
(Fig 1) .25/200 um MESFET



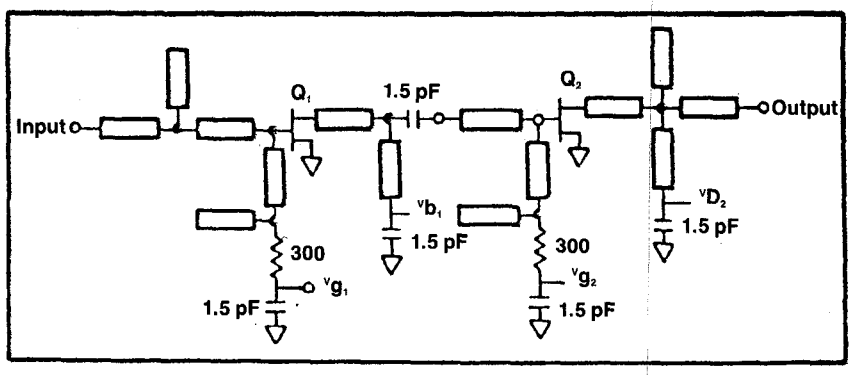
(Fig 2) Equivalent Circuit



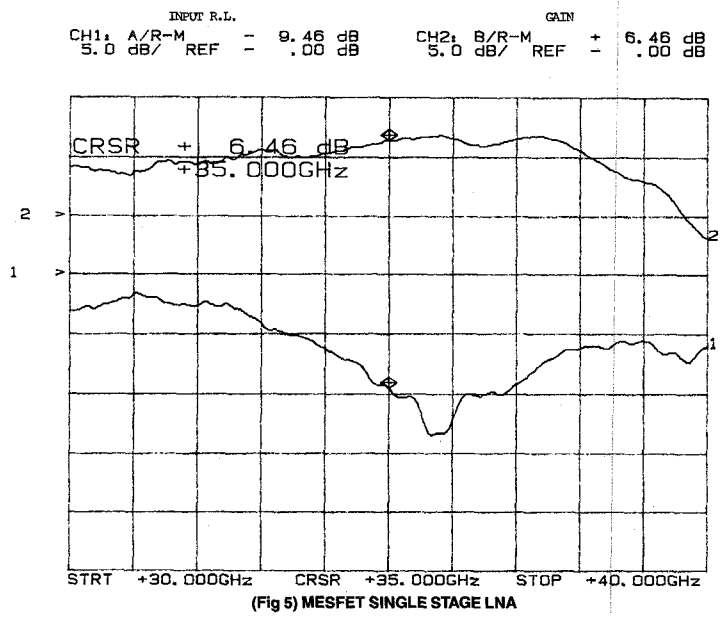
(Fig 3a) Single Stage LNA



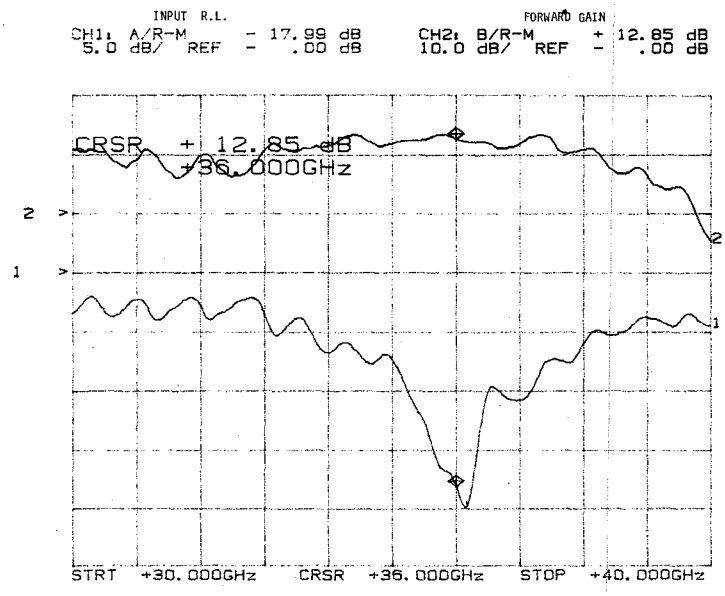
(Fig 3b) Two Stage LNA



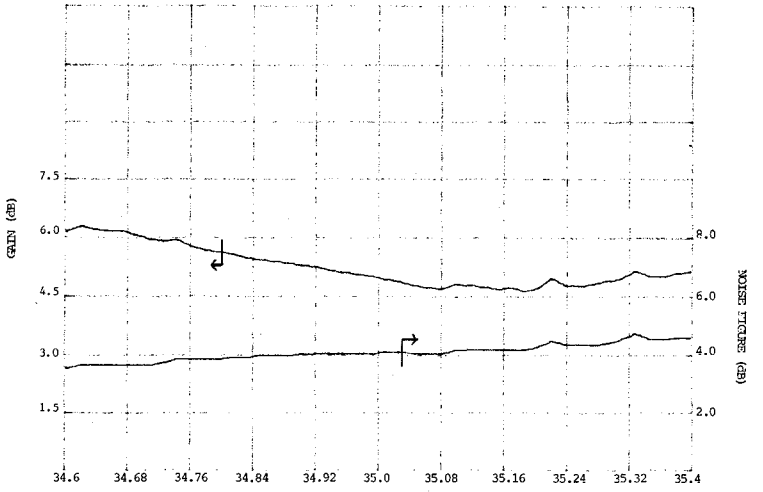
(Fig 4) Two Stage LNA Schematic Diagram



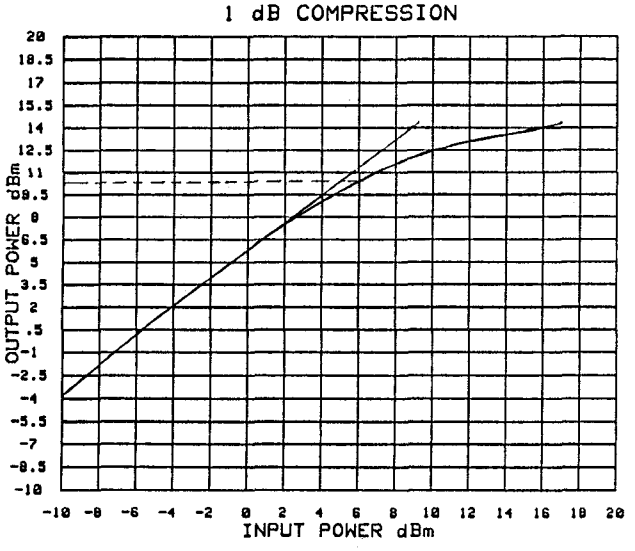
(Fig 5) MESFET SINGLE STAGE LNA



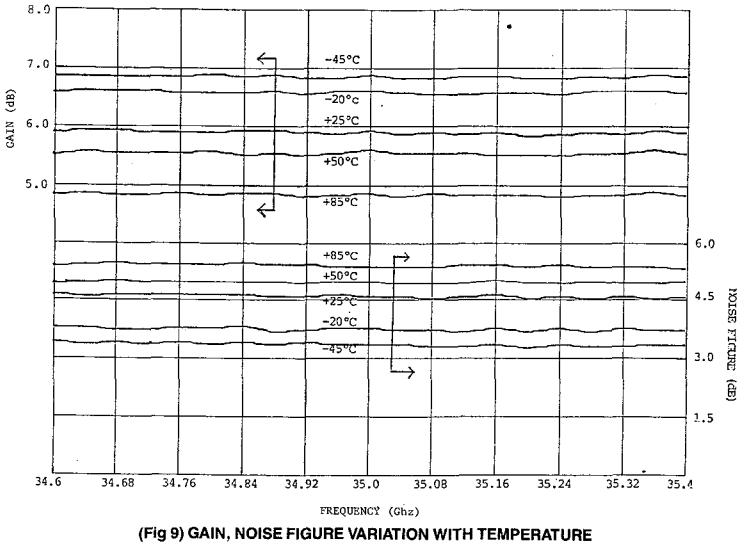
(Fig 6) MESFET TWO STAGE MONOLITHIC LNA



(Fig 7) MESFET S/S LNA GAIN, NF vs. FREQ (GHz)



(Fig 8) Po @ 1 dB gain compression



(Fig 9) GAIN, NOISE FIGURE VARIATION WITH TEMPERATURE

best noise figure consistent with an input/output VSWR less than 2 to 1. Noise analysis is performed using Fukui noise model as modified by Podell (2). Noise parameters of several devices from different wafers were measured in the frequency range 12 to 18 GHz. Knowing these noise parameter values, the 'K' factors described in the Fukui noise equations were derived. As a next step, we calculated the device noise parameters in the Ka-band and thereby deduced the input impedance value for best noise match. A matching network consisting of an open shunt stub and a cascaded transmission line is used to transform this impedance to 50 ohms. For the two-stage amplifier, we have synthesized a suitable interstage matching network to provide match between the output impedance of the first stage and input impedance of the second stage.

The single and two-stage monolithic LNA chips are shown in Figure 3. The two-stage LNA circuit schematic is shown in Figure 4. These designs are realized on a 60 x 70 mils and 85 x 75 mils size chip, respectively. The chip thickness is 4 mils. Low frequency stability is improved by using epi resistors in the gate bias circuit which is bypassed using radial quarter wave stubs in order not to affect the noise performance at the frequency of interest.

AMPLIFIER TEST RESULTS

The single-stage and dual-stage amplifiers have been tested using in-house test fixture. The test fixture with coaxial connectors and with 50 ohm quartz lines at the input and output have measured repeatedly an insertion loss of .35 dB and return loss of 20 dB. The single and cascaded two-stage MESFET amplifiers have produced 6.5 dB and 12.85 dB gain when biased at 50% Idss as shown in Figures 5 and 6. Power output at 1 dB gain compression is 10 dBm as depicted in Figure 8. The single state amplifier under optimum bias conditions yielded 4 dB noise figure at 35 GHz (Figure 7), while the dual stage produced 6 dB NF with 10.5 dB associated gain. This corresponds to device noise figure of 3 dB at 35 GHz. We evaluated these amplifiers for gain and noise figure variation with temperature from -45°C to +85°C and the results are shown in Figure 9. We observe that a gain and NF margin of 1.5 dB is needed to achieve the nominal performance over the entire temperature range. For this reason, we are currently evaluating devices with enhanced gate cross sectional areas. These 'mushroom' shaped gates are fabricated using our E-beam lithography system and a trilevel resist structure.

CONCLUSION

A monolithic LNA operating at 35 GHz using quarter micron MESFET device has been designed to yield high level performance that rivals the previously published HEMT results. This performance should pave way for system level integration at Ka-band frequencies with lower material costs and higher process yields.

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